

Precision MDSD Digital Processor DC-950



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In 2000, Accuphase launched the SA-CD/CD Digital Processor DC-101 as the legendary Separate SA-CD/CD Player System.

After that, Accuphase launched DC-801 in 2006 and DC-901 in 2011 with developing epoch-making technologies like MDSD(Multiple Double Speed DSD).

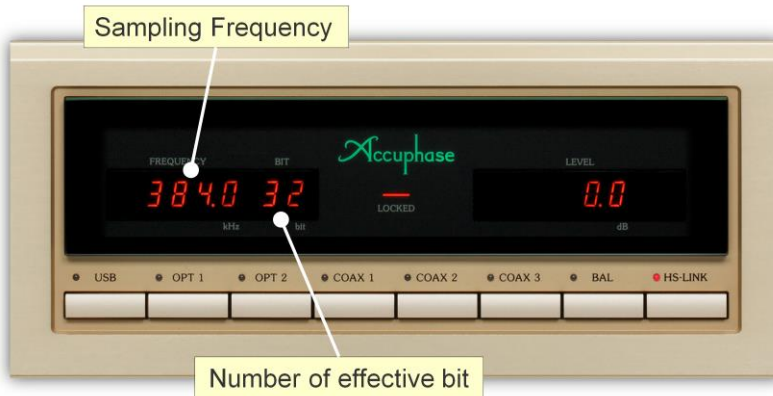
Now, Accuphase makes DC-950 known to the public, which is the 4th generation separate SA-CD/CD digital processor succeeding DC-901.

Main technical features of DC-950 are...

- Ultra Low Noise
- Installation of high-quality digital interface HS-LINK Ver.2.

Front display

- Easy to see: Sampling Frequency & Number of Effective Bits



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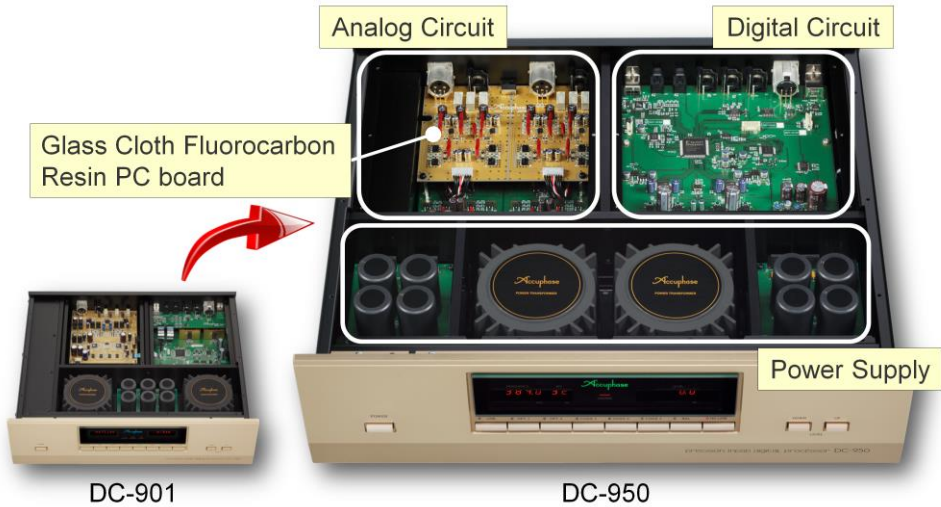
DC-950 has refined the numeral display from the former model.

DC-950 newly applies 7-segment LED instead of previous dot matrix LED, this new LED allows DC-950 to achieve much better visibility with large character display.

DC-950 is now possible to show sampling frequency and the number of effective bits of input signals on front panel display.

Internal view

- Advanced Symmetrical Layout



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DC-950 realizes further-advanced symmetrical layout.

On the back panel side, the digital circuit is right, and the analog circuit is left. The analog filter sections are mounted on Glass Cloth Fluorocarbon Resin(commonly known as “Teflon”) PC board.

On the front panel side, strong power supplies are disposed for completely separate construction of analog and digital sections, each powered by a high-efficiency toroidal transformer.

Electrical Performance

- Ultra Low Noise



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Ultra Low Noise is one of the main technical features of DC-950.

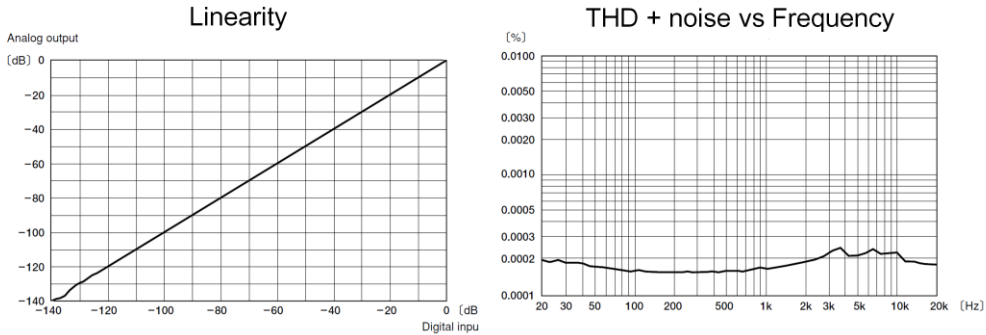
The former model, DC-901 has excellent noise performance, however, DC-950 achieves 20% lower output noise voltage than even DC-901.

DC-950 guarantees,

SN ratio: 122dB(it means that 2.0 μV of output noise voltage)

Electrical Performance

- Ultra linear
- Ultra low THD+noise



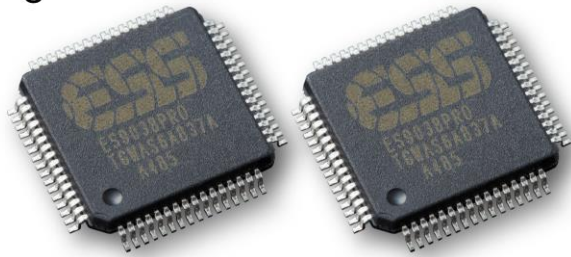
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DC-950 proudly shows the great linearity and THD+noise characteristics which are quite important for music playbacks, and this clearly proves DC-950 has the world class electrical performance.

D/A converter

- 8 parallel D/A converters per channel
 - ES9038PRO 32bit HyperStream DAC,
1 chip per channel
 - MDS++ for PCM signal
 - MDSD for DSD signal



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For D/A Converter section, Accuphase newly adopts ESS Technology's 32bit Hyperstream DAC ES9038PRO. Each channel uses 1 DAC chip which incorporates 8 converters, and has them drive in parallel.

The former model DC-901 has 2 chips of ESS Technology's DAC ES9018S per channel. Each chip incorporates 8 converters, resulting in having 16 converters drive in parallel.

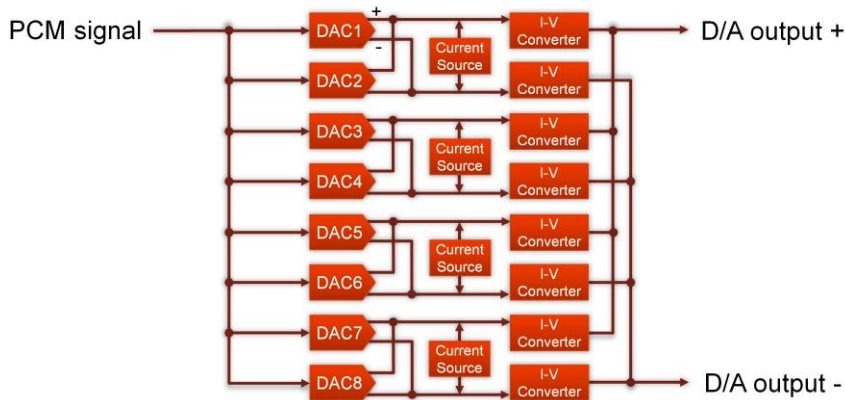
Although the number of paralleled DACs seems to be cut by half, ES9038PRO has 4 times larger output current than ES9018S. Therefore, it follows that DC-950 DAC section has 2 times larger output current than DC-901.

Accuphase establishes this 8-circuit parallel drive as the optimal solution to bring out their best electrical performances.

These DACs are essential for our original circuits, MDS++ for PCM signal and MDSD for DSD signal.

Multiple Delta-Sigma++

- Technique to make DAC parallel
- Performances improved by a factor of 2.8



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MDS++ is a technique to make DACs parallel.

The same digital signal is supplied to each converter. The output of each DAC is combined.

The Audio signal values are added up. But the conversion error and noise are canceled.

The ratio between the signal and conversion errors increases. So the converter performance is improved.

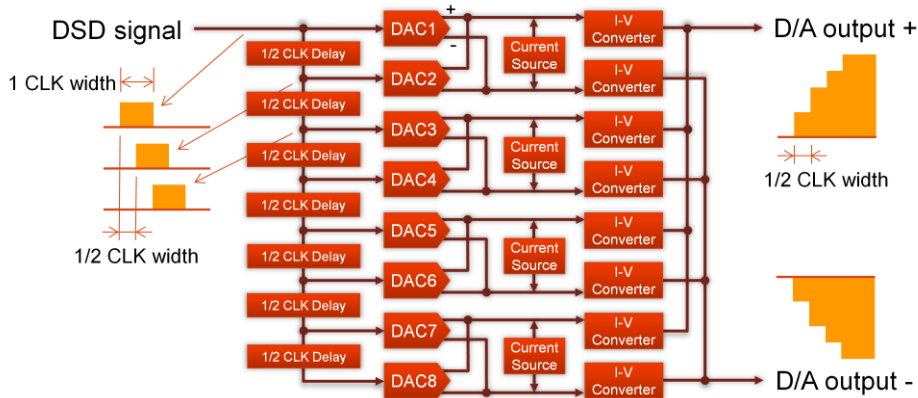
The improvement degree works by a square root of the number of DACs.

In DC-950, all performances are improved by a factor of 2.8.

As the output current of D/A Converters is very large, the number of I/V converters are increased to 4 circuits each at \pm output from 1 circuit each in DC-901.

Multiple Double Speed DSD

- In the high freq. works as a low pass filter, in the low freq. works as MDS++ principle



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MDSD stands for Multiple Double Speed DSD.

The DSD signal has a big noise in the high frequency. It must be removed.

MDSD works as a low pass filter to remove the noise in the high frequency and also works as the MDS++ principle to improve the characteristics in the low frequency.

The point of MDSD is the delay elements.

DSD signal in DC-950 is D/A converted with half-delayed clocks and is combined when it comes to the output.

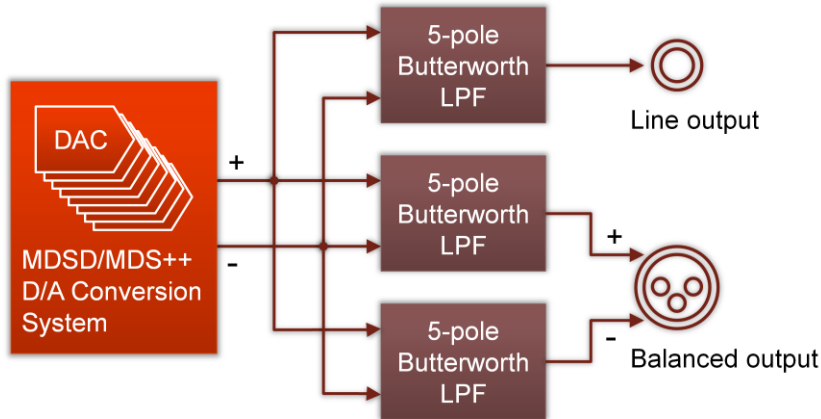
As the analog output becomes half-clock time resolution, it allows double speed operation.

This configuration is a moving-average filter.

It works as a complete linear phase low pass filter and removes high frequency noise of DSD signal.

Direct Balanced Filter

- Balanced connected independence post filters



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Full-balanced structure is employed after D/A converter section in DC-950.

In addition, the independent low pass filter is installed for each audio output.

Due to this, the sound signals from all the outputs become high quality.

Digital Inputs

- HS-LINK
 - Version1: 192kHz/24bit, 2.8224MHz/1bit
 - Version2: 384kHz/32bit, 5.6448MHz/1bit
- Balanced, Coaxial: 192kHz/24bit
- Optical: 96kHz/24bit
- USB2.0: 384kHz/32bit, 11.2896MHz/1bit



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DC-950 is equipped with 5 kinds of 8 digital inputs. USB Input accepts 384kHz/32bit-PCM or 11.2896MHz-DSD. DSD data can be received both DoP (DSD over PCM) and ASIO2.1.

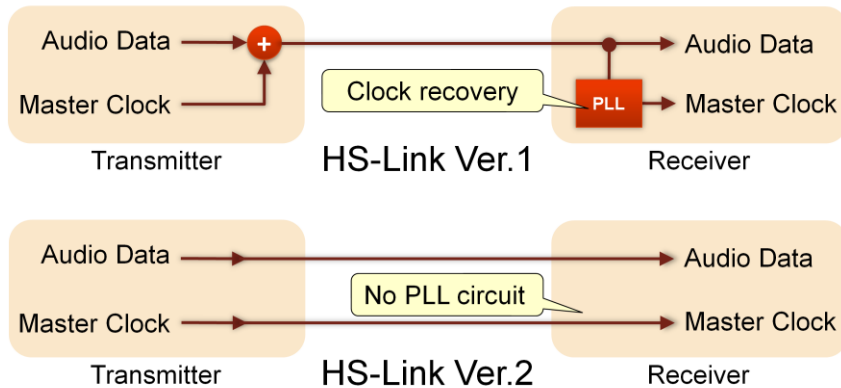
HS-LINK has been evolved as Version2.

Original HS-LINK(Ver.1) transmits and receives only 192kHz/24bit-PCM or 2.8224MHz-DSD, but Ver.2 comes to be able to transmit and receive 384kHz/32bit-PCM, 5.6648MHz-DSD.

DC-950 automatically recognizes either Ver.1 or Ver.2 transmissions.

HS-Link Version2 advantages

- Transmitting the master clock separately
 - No Jitters occurred from Clock Recovery circuit



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The biggest feature of HS-Link Ver.2 is sending the music signal and the master clock separately to D/A converter in a receiver.

HS-LINK Ver.1 sends the music signal merging the master clock together, PLL circuit master clock recovery is needed at receiver side.

Since master clock is been transmitting as it is, in HS-LINK Ver.2, not only master clock recovery is unnecessary at receiver side but it is freed from the jitter at PLL clock recovery circuit.